Remarks/Arguments

Applicant has reviewed and carefully considered the Office Action mailed on March 1, 2010. Applicant has amended claim 8 for clarity purposes. Claims 7 and 9 remain canceled without prejudice. Applicant appreciates the allowance of claims 5, 6, 13 and 14 and the allowability of claims 8, 10 and 15-16 if amended to overcome the rejections under 35 U.S.C. §112, second paragraph. Claims 1-6, 8 and 10-16 remain pending in this application. Applicant requests reconsideration of the above-identified application in view of the following remarks.

Rejections under 35 U.S.C. §112, second paragraph

Claims 8, 10 and 15-16 stand rejected under 35 U.S.C. §112, second paragraph for purportedly lacking clarity due to the use of conditional "if" statements in claim 8. In particular, the Office Action asserts that it is unclear as to whether reference signals are applied to both reference inputs. Applicant has amended claim 8 in a manner to overcome the rejection. As such, applicant requests withdrawal of the rejection.

Rejections under 35 U.S.C. §103(a)

Claims 1-2 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Admitted Prior Art (hereinafter 'APA'), in view of U.S. Patent No. 5,550,594 (hereinafter 'Cooper'), further in view of JP Publication No. 2000-49841A (hereinafter referred to as 'Watanabe').

Claim 1 of the present application recites, inter alia:

a first reference input;

a second reference input;

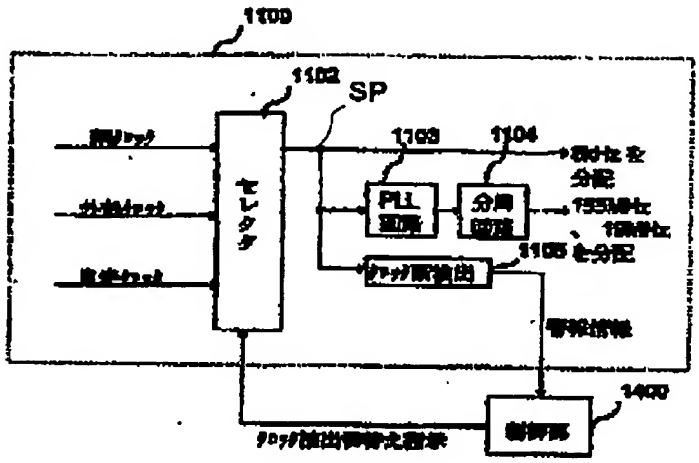
a reference select circuit coupled to said first and second reference inputs; and

at least one router component coupled to said reference select circuit;

wherein said reference select circuit: (1) passes a first signal applied to said first reference input to said at least one router component as a first reference signal and a second signal applied to said second reference input to said at least one router component as a second reference signal in response to determining that said first and second signals are error-free; (2) passes said first signal to said at least one router component as said first reference signal and as said second reference signal in response to determining that said first signal is error-free and said second signal is not error-free; and (3) passes said second signal to said at least one router component as said first reference signal and as said second reference signal in response to determining that said first signal is not error-free and said second signal is error-free.

Accordingly, claim 1 includes a reference select circuit configured to pass a first signal applied to a first reference input and a second signal applied to a second reference input (see, e.g., Specification, p. 9, lines 1-4; FIG. 2, elements 144, 146, 148). None of Watanabe, Cooper and APA, taken singly or in any combination, discloses or renders obvious this feature of claim 1.

For example, Watanabe discloses a selector 1102 within a clock board 1100 that selects between three different input signals to output a single signal, as shown in Drawing 9. Further, Drawing 10, reproduced below, provides a more detailed illustration of the clock board 1100, and indicates that the selector 1102 selects one signal among three input signals for output and splits the selected signal for distribution to three other components.



Accordingly, Watanabe does not disclose or render obvious passing a first reference input and a second signal applied to a second reference input. Rather, as discussed above, Watanabe discloses passing only one of the three input signals.

In support of the rejection, the Office Action cites paragraph 0005 of Watanabe to assert that the passing of two reference signals. The examiner relies on this excerpt to support the following assertion:

> In drawing 10, 3 mentioned above 8 kHz clocks are chosen through the selector (IC) 1102 within the clock board 1100, and *the selected clock, dividing generation is carried out* in what is then distributed to each of other substrate in the switchboard 100 as an 8 kHz clock, and PLL circuit 1103 and the frequency divider 1104 at various frequency, and it is distributed to each of other same substrate in the switchboard 100 . . . For example, when *the network clock is chosen* by the selector 1102 and a clock stop occurs, the control section 1400 is performing processing which chooses 8 kHz of running by oneself clock by the selector 1102 after malfunction detection. (Watanabe translation, paragraph. 5) (emphasis added).

In particular, the Examiner seems to rely on the first sentence, stating that "3 mentioned above 8 kHz clocks are chosen through the selector (IC) 1102."

However, in the context of the passage, when read as a whole with reference to the accompanying figure, the clause concerning "chosen" clocks means that the selector chooses one of the three clock signals, as opposed to choosing all three of the clock

signals for output. For example, in the same clause, Watanabe refers to *the* selected clock, indicating that choice of a ***single*** clock for distribution. In addition, the passage also notes the division of the selected clock for distribution to other circuit components, consistent with the explanation of Drawing 10 provided above. Furthermore, the end of the passage provides that, "if a network clock is chosen by the selector and a malfunction occurs, then a different clock 8 kHz chosen, further indicating the selection of a ***single*** clock. Moreover, the drawings themselves, as discussed above, clearly indicate selection of one output signal from three input signals (see 1102 in Drawing 10 above).

Accordingly, applicants respectfully submit that Watanabe does not disclose or render obvious a reference select circuit that passes a first signal applied to a first reference input and a second signal applied to a second reference input.

Further, applicants respectfully submit that Cooper does not cure the deficiencies of Watanabe. In support of the rejection of claim 1, the Office Action cites a video switch in the Z section of U435 of FIG. 21 as teaching the use of one signal in lieu of another signal. However, similar to Watanabe, the video switch does not pass both reference signals. For example, as shown in FIG. 21, the Z section of U435 includes a first input Z0 corresponding to a reference signal and a second input Z1 corresponding to an input video signal. In particular, Cooper teaches that if the reference signal at Z0 is missing, the video input signal Z1 appear at the output at Z (see, e.g., Cooper, column 16, lines 25-28) (see also Cooper, column 4, lines 34-38). However, nowhere does Cooper teach that the Z section selector passes both the input video signal and the reference signal. Furthermore, for completeness, applicants note that the purported APA also does not teach this feature.

Accordingly, claim 1 patentably distinguishes over the Watanabe, Cooper and/or APA at least because they do not disclose or render obvious a reference select circuit configured to pass a first signal applied to a first reference input and a second signal applied to a second reference input, as recited in claim 1. In addition, applicant submits that claim 2 patentably distinguishes over Watanabe, Cooper and/or APA due at least to its dependency from claim 1. As such, applicant requests withdrawal of the rejection of claim 2.

Claims 3 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of Cooper in further view of Watanabe in further view of U.S. Patent No. 6,680,939 (hereinafter 'Lydon'). Claims 3 and 4 depend from claim 1, and as such, incorporate by reference all of the features of claim 1. Thus, claims 3 and 4 incorporate by reference a select circuit configured to pass a first signal applied to a first reference input and a second signal applied to a second reference input. As discussed above, Watanabe, Cooper and/or APA fail to disclose or render obvious this feature of applicant's claim 1. Moreover, Lydon fails to cure the deficiencies Watanabe, Cooper and/or APA, as Lydon nowhere discloses manipulating reference signals in any way. Accordingly, claims 3 and 4 patentably distinguish over the cited references. Applicant requests withdrawal of the rejection and allowance of the claims.

Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of Cooper in further view of Watanabe and in further view of U.S. Publication No. 2002/0031148 (hereinafter 'Watanabe '148').

Claim 11 depends from claim 1 and, as such, incorporates by reference the features recited therein. Accordingly, claim 11 includes a reference select circuit configured to pass both a signal applied to a first reference input and a signal applied to a second reference input. As discussed above, Watanabe, Cooper and/or APA do not disclose or render obvious this feature.

Moreover, Watanabe '148 does not cure the deficiencies of Watanabe, Cooper and APA. Similar to Cooper, the selector of Watanabe passes only one of the two signals it receives. The selector never passes both received signals (see, e.g., Watanabe, FIG. 1, 'SEL'). Thus, claim 11 patentably distinguishes over Watanabe, Cooper, APA and/or Watanabe '148, taken singly or in any combination, at least because the references do not disclose or render obvious a reference select circuit that passes both signals applied to a first reference input and signals applied to a second reference input, as recited in clause (1) of claim 1. As such, applicant requests withdrawal of the rejection of claim 11.

Claim 12 stands rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of Cooper in further view of Watanabe and in further view of "Is Your Plant Infrastructure Up To Handling Multichannel Digital Audio?" (hereinafter 'the Bytheway publication').

Claim 12 is dependent from claim 1 and, as such, claim 12 includes a reference select circuit that is configured to pass a first signal applied to a first reference input and a second signal applied to a second reference input. As discussed above, APA, Cooper, and/or Watanabe do not disclose or render obvious at least this feature. Similarly, the Bytheway publication fails to cure the deficiencies the references. While the Bytheway publication generally describes synchronizing input signals to a common reference signal, Bytheway does not disclose the use of a reference select circuit. Accordingly, claim 12 patentably distinguishes over the cited references for at least the reasons discussed above. Applicant requests withdrawal of the rejection of claim 12.

Conclusion

In view of the foregoing, applicants solicit entry of this amendment and allowance of the claims. If the Examiner cannot take such action, the Examiner should contact the applicant's attorney at (609) 734-6820 to arrange a mutually convenient date and time for a telephonic interview.

No fees are believed due with regard to this Amendment. Please charge any fee or credit any overpayment to Deposit Account No. **07-0832.**

Respectfully submitted,
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